## VERSION WITH MARKINGS TO SHOW CHANGES MADE

**In the Claims:**

**Claim 1 has been amended as follows:**

1. Apparatus for a service node used in a multimedia network comprising:

a data distributor circuit;

a data port adapted to couple [for coupling] with a data stream, said data distributor circuit having a relational code adapted to determine [for determining] whether an address field of a data packet from said data stream is intended for local distribution by said distributor [ion] circuit, wherein said data port is operably coupled to said data distributor circuit; and

a decoder in communication with said distributor [ion] circuit, said decoder having a virtual channel filter for filtering said address field to route said data packet to at least one data port.

**Claim 2 has been amended as follows:**

2. The apparatus of Claim 1 further comprising[:] an incorporator circuit electrically-coupled to said data port adapted to insert an address value having a relational code and a virtual channel code in a data input from said at least one data port, said incorporator adapted to insert [for inserting] said data input into said data stream.

**Claim 3 has been amended as follows:**

3. The apparatus of Claim 2 wherein said incorporator circuit is operably coupled with said decoder adapted to receive [for receiving] said data input.

**Claim 4 has been amended as follows:**

4. The apparatus of Claim 3 wherein said incorporator circuit comprises[:] a Field Programmable Gate Array adapted to execute [executing] a firmware routine adapted to insert [for inserting] said address value into said data input[,] and adapted to insert [for inserting] said data input into said data stream.

**Claim 5 has been amended as follows:**

5. The apparatus of Claim 1 wherein said data distributor circuit comprises[:] a Field Programmable Gate Array adapted to execute [executing] a firmware routine adapted to filter [for filtering] said data stream with respect to said relational code.

**Claim 6 has been amended as follows:**

6. The apparatus of Claim 5 wherein said data stream is a data cell-based data stream having a plurality of data packets.

**Claim 7 has been amended as follows:**

7. A multimedia network card comprising:

a deserializer coupled to a serial data stream, said deserializer adapted to convert [for converting] said serial data stream to a parallel data stream representing a plurality of data of said serial data stream;

a receiver coupled to said deserializer, said receiver having a relational code adapted to determine [for determining] whether an address field of said parallel data stream designates local distribution;

a decoder in communication with said receiver, said decoder having a virtual channel filter adapted to filter [for filtering] said address field to route said data packet to at least one data port; and

a serializer coupled to said receiver, said serializer adapted to convert [for converting] an output data stream from said receiver into an output serial data stream.

**Claim 8 has been amended as follows:**

8. The multimedia network card of Claim 7 further comprising:

an incorporator coupled to said decoder, said incorporator adapted to insert an address value having a relational code and a virtual channel code in a data input from said at least one data port, said incorporator adapted to insert [for inserting] said data input into said data stream; and

a second serializer coupled to said receiver, said second serializer adapted to convert [for converting] an output data stream from said receiver into an output serial data stream.

**Claim 9 has been amended as follows:**

9. The multimedia network card of Claim 8 further comprising[:] a second deserializer coupled to said incorporator and said serial data stream, said second deserializer adapted to convert [for converting] a parallel data stream into a serial data stream such that said incorporator is adapted to provide [provides] a redundant receiver function to said receiver.

**Claim 10 has been amended as follows:**

10. The multimedia network card [apparatus] of Claim 9 wherein said incorporator circuit comprises[:] a Field Programmable Gate Array adapted to execute [executing] a firmware routine adapted to insert [for inserting] said address value into said data input[,] and adapted to insert [for inserting] said data input into said data stream.

**Claim 11 has been amended as follows:**

11. The multimedia network card [apparatus] of Claim 10 wherein said receiver comprises[:] a Field Programmable Gate Array adapted to execute [executing] a firmware routine adapted to filter [for filtering] said data stream with respect to said relational code.

**Claim 12 has been amended as follows:**

12. The multimedia network card [apparatus] of Claim 11 wherein said data stream is a data cell-based data stream having a plurality of data packets.

**Claim 13 has been amended as follows:**

13. A method of interfacing an multimedia communications data stream having a plurality of data packets, the method comprising:

(a) receiving [inputting] a data packet of the plurality of data packets [data stream];

(b) determining whether an address field of the data packet is intended for local distribution;

(c) routing the data packet to a data port if the data packet is intended for local distribution; and

(d) returning the data packet to the data stream if the data packet is not intended for local distribution.

**Claim 14 has been amended as follows:**

14. The method of Claim 13 further comprising the step[s] of:

(e) incorporating a data packet from a local data port into the data stream for transmission. [The method of Claim 13 further comprising the steps of: (e) repeating steps (a) through (d) for a plurality of data packets].

**Claim 15 has been amended as follows:**

15. The method of Claim 14[3] further comprising the steps of:

(f[e]) repeating steps (a) through (e[d]) for the plurality of data packets. [The method of Claim 13 further comprising the steps of: (e) incorporating a data packet from a local data port into the data stream for transmission.]

**Claim 16 has been added as follows:**

16. A photonic area network adapted to distribute a plurality of data bandwidth segments from a plurality of external networks to a plurality of peripheral devices, the photonic area network comprising:

a wide-signal bandwidth multi-access channel;

a head-end communications circuit adapted to format the data bandwidth segments into a multiplexed signal transmittable via the wide-signal bandwidth multi-access channel, wherein the head-end communications circuit comprises a bi-directional interface operably coupled to the external networks and to the multi-access channel;

a plurality of set top box circuits each comprising:

a microcontroller containing memory; and

a peripheral device interface operably coupled to the plurality of peripheral devices adapted to process the data bandwidth segments, wherein each of the set-top box circuits are operably coupled, in a ring network configuration, to the multi access channel; and;

a program, executed by the set-top box microcontroller, adapted to route the data bandwidth segments according to a software subscription table stored in the memory.

**Claim 17 has been added as follows:**

17. The photonic area network of claim 16, wherein the data bandwidth segments include at least one of: television programming data, audio programming data, video data, computer data and telephony service data.

**Claim 18 has been added as follows:**

18. The photonic area network of claim 16, wherein the program is adapted to aggregate a multiplexed set of the data bandwidth segments to be transmitted to a subsequent one of the set-top box circuits.

**Claim 19 has been added as follows:**

19. The photonic area network of claim 16, wherein the multi-access channel comprises a plurality of units each including:

an optical detector circuit adapted to receive photonic signals representative of a transmittable signal; and

an optical laser transmit circuit adapted to transmit photonic signals representative of the signal, wherein the units are operably coupled to the head-end communications circuit and a subsequent set of the units forming a ring network.

**Claim 20 has been added as follows:**

20. The photonic area network of claim 19, wherein each of the plurality of units further comprise:

a first beamsplitter comprising a first surface aligned with the optical detector circuit; and

a second optical laser transmit circuit aligned with a second surface of the first beamsplitter.

**Claim 21 has been added as follows:**

21. The photonic area network of claim 20, wherein each of the plurality of units further comprise:

a second beamsplitter comprising a first surface aligned with the optical laser transmit circuit; and

a second optical detector circuit aligned with a second surface of the second beamsplitter.

**Claim 22 has been added as follows:**

22. The photonic area network of claim 20, wherein each of the plurality of units further comprise:

an optical window comprising a top edge and a bottom edge;

an enclosure coupled to the top edge of the optical window; and

a bottom plate coupled to the bottom edge of the optical window, wherein the optical laser transmit circuit and the optical laser detector circuit of each of the units are protected.

**Claim 23 has been added as follows:**

23. The photonic area network of claim 16, wherein the multiaccess channel comprises at least one of:

a fiber optic cable;

a data signal path of infrared form; and

a data signal path of radio frequency form.

**Claim 24 has been added as follows:**

24. The photonic area network of claim 16, wherein the head-end communications circuit further comprises:

a signal formatting circuit, operably coupled to a unidirectional television channel source comprising carrier signals, adapted to synchronize the carrier signals for combination with the signal;

a channel selection register adapted to designate a core television channel selection, wherein the channel selection register is operably coupled to the signal formatting circuit;

a demultiplexer adapted to convert the multiplexed data signal into the data bandwidth segments; and

a multiplexer adapted to multiplex the unidirectional television channel source and the plurality of external networks into the multiplexed data signal, wherein the multiplexer and the demultiplexer are operably coupled to the signal formatting circuit.

**Claim 25 has been added as follows:**

25. The photonic area network of claim 24, wherein the head-end communications circuit further comprises a head-end microcontroller:

adapted to monitor voice and data transmitted from the demultiplexer; and

adapted to route the data bandwidth segments to the multiplexer for combination with the plurality of external networks into the multiplexed data signal, wherein the head-end microcontroller is operably coupled to the plurality of external networks and to the channel selection register.

**Claim 26 has been added as follows:**

26. The photonic area network of claim 25, wherein the head-end communications circuit further comprises a computer operably coupled to the channel selection register and the microcontroller for executing a program which creates and maintains a master scheduling plan of television channels and billing services.

**Claim 27 has been added as follows:**

27. The photonic area network of claim 16, wherein the set-top box circuit further comprises:

a television switch select adapted to designate video and audio data;

a demultiplexer adapted to convert the multiplexed signal into a set of data bandwidth segments;

a multiplexer adapted to combine a plurality of the video and audio data into the multiplexed signal wherein the multiplexer is operably coupled to the television switch select and to the demultiplexer; and

a set-top box microcontroller comprising an interface operably coupled to at least one of a plurality of peripheral devices, wherein the set-top box microcontroller is adapted to direct a plurality of user data from the demultiplexer to the multiplexer via the plurality of peripheral devices for combination with the plurality of video and audio data into the multiplexed signal, wherein the set-top box microcontroller is operably coupled to the demultiplexer and the multiplexer.

**Claim 28 has been added as follows:**

28. A method for interfacing an external communications source comprising a plurality of data bandwidth segments with a plurality of peripheral devices, the method comprising:

receiving the plurality of data bandwidth segments;

combining the plurality of data bandwidth segments into a multiplexed data signal;

transmitting the multiplexed data signal as photonic energy;

receiving the multiplexed data signal;

demultiplexing the received multiplexed data signal into the data bandwidth segments;

routing the demultiplexed data bandwidth segments according to a software routing table;

accepting bi-directional data from one of the peripheral devices;

combining the bi-directional data with unidirectional data into a subsequent multiplexed data signal; and

transmitting the subsequent multiplexed signal as photonic energy.

**Claim 29 has been added as follows:**

29. A wide-signal bandwidth multi-access channel comprising a plurality of units each including:

a first circuit adapted to receive photonic signals representative of a transmittable signal; and

a second circuit adapted to transmit multiplexed photonic signals representative of a multiplexed data signal, wherein the units are operably coupled to a third circuit and a subsequent set of the units, wherein such coupling provides a ring network configuration.

**Claim 30 has been added as follows:**

30. The wide-signal bandwidth multi-access channel of claim 29, wherein each of the plurality of units further comprise:

a first module comprising a first surface aligned with the second circuit; and

another second circuit aligned with a second surface of the first module.

**Claim 31 has been added as follows:**

31. The wide-signal bandwidth multi-access channel of claim 29, wherein each of the plurality of units further comprise:

a second module comprising a first surface aligned with the second circuit; and

another second circuit aligned with a second surface of the second module.

**Claim 32 has been added as follows:**

32. The wide-signal bandwidth multi-access channel of claim 29, wherein each of the plurality of units further comprise:

an optical window comprising a top edge and a bottom edge;

an enclosure coupled to the top edge of the optical window; and

a bottom plate coupled to the bottom edge of the optical window, wherein the first circuit and the second circuit of each of the units are protected.

**Claim 33 has been added as follows:**

33. The wide-signal bandwidth multi-access channel of claim 29, wherein the wide-signal bandwidth multi-access channel consists of a fiber optic cable.

**Claim 34 has been added as follows:**

34. The wide-signal bandwidth multi-access channel of claim 29, wherein the wide-signal bandwidth multi-access channel consists of an infrared data signal path.

**Claim 35 has been added as follows:**

35. The wide-signal bandwidth multi-access channel of claim 29, wherein the wide-signal bandwidth multi-access channel consists of a radio frequency data signal path.

**Claim 36 has been added as follows:**

36. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals comprise a multiplexed data carrier signal comprised of Ethernet packets.

**Claim 37 has been added as follows:**

37. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals comprise multiplexed data carrier signals comprised of Frame Relay packets.

**Claim 38 has been added as follows:**

38. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals are frequency domain multiplexed (FDM) signals.

**Claim 39 has been added as follows:**

39. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals use On-Off Keying waveforms.

**Claim 40 has been added as follows:**

40. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals use Frequency-Shift Keying waveforms.

**Claim 41 has been added as follows:**

41. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals use Quadrature-Phase-Shift Keying waveforms.

**Claim 42 has been added as follows:**

42. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals use Quadrature-Amplitude-Modulation waveforms.

**Claim 43 has been added as follows:**

43. The wide-signal bandwidth multi-access channel of claim 29, wherein the photonic signals use a proprietary modulation.

**Claim 44 has been added as follows:**

44. A head-end communications circuit adapted to format data bandwidth segments into a signal transmittable via a wide-signal bandwidth multi-access channel, wherein the head-end communications circuit comprises a bi-directional interface operably coupled to external networks and to the multi-access channel, the head-end communications circuit comprising:

a signal formatting circuit, operably coupled to a unidirectional television channel source comprising carrier signals, adapted to synchronize the carrier signals for combination with the signal; and

a channel selection register adapted to designate a core television channel selection, wherein the channel selection register is operably coupled to the signal formatting circuit.

**Claim 45 has been added as follows:**

45. The head-end communications circuit of claim 44 further comprising:

a demultiplexer adapted to convert the signal into the data bandwidth segments; and

a multiplexer adapted to multiplex the unidirectional television channel source and a plurality of external networks into the signal, wherein the multiplexer and the demultiplexer are operably coupled to the signal formatting circuit.

**Claim 46 has been added as follows:**

46. The head-end communications circuit of claim 45 further comprising a head-end microcontroller adapted to:

monitor voice and data transmitted from the demultiplexer; and

route the data bandwidth segments to the multiplexer for combination with the plurality of external networks into the multiplexed data signal, wherein the head-end microcontroller is operably coupled to the plurality of external networks and to the channel selection register.

**Claim 47 has been added as follows:**

47. The head-end communications circuit of claim 46 further comprising a computer operably coupled to the channel selection register and the microcontroller for executing a program which creates and maintains a master scheduling plan of television channels and billing services.

**Claim 48 has been added as follows:**

48. The head-end communications circuit of claim 44 further adapted to dynamically allocate a transmission rate of the data bandwidth segments based on a user demand.

**Claim 49 has been added as follows:**

49. The head-end communications circuit of claim 44 further adapted to route the data bandwidth segments addressed to nodes on the multi-access channel, wherein the data bandwidth segments are unidirectional and bi-directional.

**Claim 50 has been added as follows:**

50. The head-end communications circuit of claim 44 further comprising a data compression/decompression circuit for compressing and decompressing the data bandwidth segments.

**Claim 51 has been added as follows:**

51. The head-end communications circuit of claim 44 further comprising system failure monitoring and recovery functions.

**Claim 52 has been added as follows:**

52. The head-end communications circuit of claim 44 further comprising software adapted to approve user access to the multi-access channel.

**Claim 53 has been added as follows:**

53. The head-end communications circuit of claim 52, wherein the software is adapted to allocate the user access to the multi-access channel.

**Claim 54 has been added as follows:**

54. A set-top box circuit comprising:

a module adapted to designate video and audio data;

a demultiplexer adapted to convert a multiplexed signal into a set of data bandwidth segments;

a multiplexer adapted to combine a plurality of the video and audio data into the multiplexed signal, wherein the multiplexer is operably coupled to the module and to the demultiplexer; and

a set-top box microcontroller comprising an interface operably coupled to at least one peripheral device, wherein the set-top box microcontroller is adapted to direct a plurality of user data from the demultiplexer to the multiplexer via a plurality of peripheral devices for combination with the plurality of video and audio data into the multiplexed signal wherein the set-top box microcontroller is operably coupled to the demultiplexer and the multiplexer.

**Claim 55 has been added as follows:**

55. A plurality of set-top box circuits each comprising:

a microcontroller containing memory; and

a peripheral device interface operably coupled to a plurality of peripheral devices adapted to process data bandwidth segments, wherein each of the set-top box circuits are operably coupled, in a ring network configuration, to a multi access channel.

**Claim 56 has been added as follows:**

56. The set-top box circuits of claim 55, wherein the microcontroller further comprises a software subscription table adapted to determine access rates of the data bandwidth segments.

**Claim 57 has been added as follows:**

57. The set-top box circuits of claim 56, wherein the software subscription table is further adapted to modify the access rates of the data bandwidth segments via a user command.

**Claim 58 has been added as follows:**

58. The set-top box circuits of claim 56, wherein the software subscription table is adapted to be remotely updated.

**Claim 59 has been added as follows:**

59. The set-top box circuits of claim 55, wherein the microcontroller is further adapted to loop back the data bandwidth segments upon detecting a failure.

**Claim 60 has been added as follows:**

60. The set-top box circuits of claim 55 wherein the microcontroller is further adapted to perform at least one of a following action on the data bandwidth segments from a group consisting of: dropping; forwarding; receiving and dropping; receiving and forwarding; looping back; and passing through.

**Claim 61 has been added as follows:**

61. A program, executed by a set-top box, adapted to perform at least one of a following action from a group consisting of:

routing data bandwidth segments on a wide bandwidth multi-access channel to a plurality of peripheral devices operably coupled to the set-top box according to a software subscription table;

accumulating the data bandwidth segments and routing the accumulated data bandwidth segments on the wide bandwidth multi-access channel to the plurality of peripheral devices operably coupled to the set-top box according to the software subscription table;

forwarding a multiplexed set of the data bandwidth segments addressed to subsequent set-top boxes; and

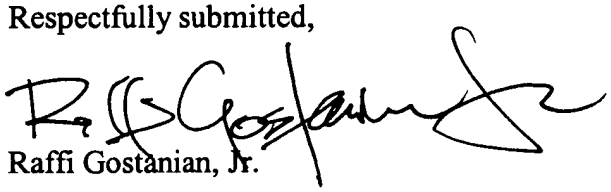
forwarding information from the plurality of peripheral devices and the data bandwidth segments addressed to subsequent set-top boxes.

**Claim 62 has been added as follows:**

62. A photonic area network comprising a multi-access channel, wherein the multi-access channel comprises sets of transmit optical lasers and receive optical detectors, wherein each of the sets are mounted substantially opposite each other and complementary arranged thereby optically coupling the sets and creating a redundant-path for an optic signal traversing the multi-access channel.

The Examiner is invited to contact the undersigned by telephone if the Examiner believes that such a communication would advance the prosecution of the present patent application.

Respectfully submitted,



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